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REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	10/764,216
Filing Date	January 23, 2004
First Named Inventor	Dale Wong
Art Unit	
Examiner Name	
Attorney Docket Number	LEOPP001C1

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☑ I hereby appoint the practitioners associated with the Customer Number: 33139

☑ Please change the correspondence address for the above-identified application to:

☑ The address associated with Customer Number: 33139

OR

☐ Firm *or* Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

☑ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	Steven Winegarden		
Name	Steven Winegarden, VP Engineering		
Date	11/1/05	Telephone	(408) 777-8090x555

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Agate Logic, Inc.

Application No./Patent No.: Patent #US 6,940,308 B2 Filed/Issue Date: September 6, 2005

Entitled: Interconnection Network For A Field Programmable Gate Array

Agate Logic, Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or

2. ☐ an assignee of less than the entire right, title and interest.
The extent (by percentage) of its ownership interest is _____ %

in the patent application/patent identified above by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: Dale Wong To: Leopard Logic, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 012769, Frame 0322 _____, or for which a copy thereof is attached.

2. From: Leopard Logic, Inc. To: Agate Logic, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel To be recorded; Frame see attached assignment, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☑ Copies of assignments or other documents in the chain of title are attached.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Steven Winegarden 11/1/05
Signature Date

Steven Winegarden (408) 777-8090 x555
Printed or Typed Name Telephone Number

V.P. Engineering
Title

ASSIGNMENT

Leopard Logic, Inc., a Delaware corporation ("Leopard"), for good and valuable consideration, receipt of which is hereby acknowledged and effective as of July 15, 2005, does hereby assign to:

AGATE LOGIC, INC.

a Cayman Islands corporation ("Assignee"), its successors, assigns and legal representatives, the entire right, title and interest in and to all subject matter of the following patent(s), patent application(s), or PCT applications of the respective countries or regions of filing:

Application Type	Application No.	Filing Date	Title
USA	**60/223,047**	**August 4, 2000**	**Interconnection Network For A Field Programmable Gate Array**
USA	**09/923,294 Patent Issued #: US 6,693,456 B2**	**August 3, 2001 Patent Issued: February 17, 2004**	**Interconnection Network For A Field Programmable Gate Array**
PCT	**PCT/US01/24445**	**August 3, 2001**	**Interconnection Network For A Field Programmable Gate Array**
EP	**01959505.7**	**August 3, 2001**	**Interconnection Network For A Field Programmable Gate Array**
USA	**10/764,216 Patent Issued #: US 6,940,308 B2**	**January 23, 2004 Patent Issued: September 6, 2005**	**Interconnection Network For A Field Programmable Gate Array**
USA	**60/279,237**	**March 27, 2001**	**Secure Intellectual Property For A Generated Field Programmable Gate Array**
USA	**10/105,874**	**March 25, 2002**	**Secure Intellectual Property For A Generated Field Programmable Gate Array**
USA	**60/307,534**	**July 24, 2001**	**Hierarchical Mux Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
USA	**10/202,397**	**July 24, 2002**	**Hierarchical Mux Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
PCT	**PCT/US02/23486**	**July 24, 2002**	**Hierarchical Multiplexer-Based Integrated Circuit Interconnect**

			Architecture For Scalability And Automatic Generation
Canada	**2454688**	**January 22, 2004**	**Hierarchical Multiplexer-Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
China	**02814980.7**	**Publication Date: October 13, 2004**	**Hierarchical Multiplexer-Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
EP	**02761162.3**	**Priority Date: July 24, 2001**	**Hierarchical Multiplexer-Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
India	**00146/CHENP/2004**	**January 23, 2004**	**Hierarchical Multiplexer-Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
Korea	**(PCT) 2004-7001008**	**January 20, 2004**	**Hierarchical Multiplexer-Based Integrated Circuit Interconnect Architecture For Scalability And Automatic Generation**
USA	**60/307,479**	**July 24, 2001**	**General Purpose Inputs And Outputs For Embedded Field Programmable Cores**
USA	**10/202,443**	**July 24, 2002**	**Inputs And Outputs For Embedded Field Programmable Gate Array Cores In Application Specific Integrated Circuits**
USA	**60/329,818**	**October 16, 2001**	**Embedded FPGA Core Interface Architecture**
USA	**10/270,022**	**October 12, 2002**	**Interface Architecture For Embedded Field Programmable Gate Array Cores**
PCT	**PCT/US02/33262**	**October 12, 2002**	**Interface Architecture For Embedded Field Programmable Gate Array Cores**
China	**02825008.7**	**June 8, 2004**	**Interface Architecture For Embedded Field Programmable Gate Array Cores**
EP	**02776229.3**	**October 12, 2002**	**Interface Architecture For Embedded Field Programmable Gate Array Cores**
USA	**60/329,892**	**October 16, 2001**	**Field Programmable Gate Array**

			Core Cell With Support For Efficient Logic Packing
USA	**10/269,830 Patent Issued #: US 6,801,052 B2**	**October 11, 2002 Patent Issued: October 5, 2004**	**Field Programmable Gate Array Core Cell With Efficient Logic Packing**
USA	**10/951,309**	**September 27, 2004**	**Field Programmable Gate Array Core Cell With Efficient Logic Packing**
PCT	**PCT/US02/32556**	**October 11, 2002**	**Field Programmable Gate Array Core Cell With Efficient Logic Packing**
China	**02824998.4**	**June 10, 2004**	**Field Programmable Gate Array Core Cell With Efficient Logic Packing**
EP	**02778523.7**	**October 11, 2002**	**Field Programmable Gate Array Core Cell With Efficient Logic Packing**
USA	**60/345,115**	**October 29, 2001**	**Programmable Cores Interface**
USA	**10/283,019 Patent Issued #: US 6,888,371 B2**	**October 29, 2002 Patent Issued: May 3, 2005**	**Programmable Interface For Field Programmable Gate Array Cores**
PCT	**PCT/US02/34634**	**October 29, 2002**	**Programmable Interface For Field Programmable Gate Array Cores**
China	**02821446.3**	**October 29, 2002**	**Programmable Interface For Field Programmable Gate Array Cores**
EP	**02773937.4**	**October 29, 2002**	**Programmable Interface For Field Programmable Gate Array Cores**
USA	**60/402,308**	**August 9, 2002**	**Single Layer Programmable Gate Array Interconnect Architecture**
USA	**10/637,749**	**August 8, 2003**	**Via Programmable Gate Array Interconnect Architecture**
PCT	**PCT/US03/24863**	**August 8, 2003**	**Via Programmable Gate Array Interconnect Architecture**
Taiwan	**92135639**	**December 16, 2003**	**Via Programmable Gate Array Interconnect Architecture**

and in and to any and all divisions, reissues, continuations and extensions thereof; and in and to all corresponding applications for Letters Patent and all Convention and Treaty Rights of any kind, in all countries throughout the world, for all such subject matter.

Leopard hereby authorize and request that the Patent Office officials in the United States, and in countries foreign to the United States, issue any and all of said Letters Patent or similar documents, when granted, to said Assignee, as the Assignee of our entire right, title and interest in and to the same, for the sole use and enjoyment of said Assignee, its successors and assigns.

Further, Leopard agree that Leopard will communicate to said Assignee, or its representatives, any facts known to me respecting said invention, and testify in any legal proceedings, sign all lawful papers, execute all divisions, continuations, substitutions, and renewal reexamination and reissue applications, execute all necessary Assignment papers to cause any and all of said Letters Patent to be issued to said Assignee, make all rightful oaths and generally do everything necessary or desirable to aid said Assignee, its successors and assigns, to obtain and enforce proper protection for said invention in the United States and everywhere else in the world.

The undersigned hereby authorizes the firm of LAW OFFICES OF EMIL CHANG to correct errors in this assignment or to insert any further identification or other information necessary or desirable to make this assignment suitable for recordal in the United States Patent Office, and any Patent Office foreign to the United States.

In Testimony Whereof, I hereunto set my hand:

Leopard Logic, Inc.

By: _____
David Tsang, Chairman